An Integrated Method For Hardware FMEA of New Electronic Products

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***Abstract*—Failure mode, effects analysis (FMEA) is widely recognized and applied in different fields, such as aviation, aerospace, automotive industries. And later FMEA has been extended to other industries, such as electronics, medical and so on. For key products, FMEA is an indispensable part in reliability analysis. However, many products are newly researched and developed, with high integrated level and complicated failure mode, reasons and effects. Historical data and similar products data are also scarce, which constrain the effectiveness of hardware FMEA. Besides, technicians are relatively young and inexperienced with incomplete understanding of failure and effects, which will result in incomplete analysis results. These problems affect implementation effect of hardware FMEA and will affect the subsequent reliability, maintainability, testability and supportability analysis work. Aiming at the above problems, this paper proposes an integrated method for hardware FMEA of new electronic products which integrates present advanced failure mode acquisition, failure mechanism analysis and failure effect analysis together. This method can effectively solve the above problems, meanwhile make supplement for the problem not taking redundant design into consideration in traditional FMEA method. It has been proved that this integrated method achieved good effect on a type of new research aviation electronic products.**

Keywords- integrated hardware FMEA; failure mode; failure simulation; failure information database

I. INTRODUCTION

As systems reliability analysis method, failure mode, effects and criticality analysis (FMEA) is proved to be effective and efficient to ensure the reliability of product. In America, Europe, Japan and other countries, after several rounds of engineering practice, FMEA is widely recognized and applied in different fields, such as aviation, aerospace, automotive industries. And later FMEA was extended to other industries, such as electronics, medical and so on. And these industries have corresponding standards, which are constantly updated, such as SAE J-1739-2009 and QS 9000 FMEA-2008 in automotive industry, IEC60812-2006[1] issued by International Electrotechnical Commission. FMEA related standards are issued and provide guide for engineering practice in different industries.

Since FMEA was introduced to China in 1980s, it has been widely used in many industries, especially in aviation and aerospace. For key products, FMEA is an indispensable part in reliability analysis. However, it is still difficult for FMEA to guide design and improvement of product effectively. Besides management reason, there are several reasons existing in application process of FMEA. First, many products are newly researched and developed, with high integrated level and complicated failure mode, reason and effects. Historical data and similar products data are also scarce. Second, presently technicians are relatively young and inexperienced with incomplete understanding of failure and effects, which will result in incomplete analysis results. These problems affect implementation effect of hardware FMEA, and will affect the subsequent reliability, maintainability, testability and supportability analysis work [2].

Aiming at the above problems, since the 1990s, lots of institutions and scholars [3~5] have taken research on establishing database with collecting failure information to assist FMEA work. In failure effects analysis, Pickard [6], Xiao [7] and Christopher [8] researched methods of multiple failure modes and effects analysis. He D [9] used Petri net to analyze multiple failure effects. Lee [10] used Bayesian net to analyze failure effects and probability of occurrence. In China, research on FMEA focused on cases analysis of fuzzy FMEA application [11~15] and cases with combination between FMEA and RAMS [18~21].

This paper proposes an integrated method for hardware FMEA of new electronic products and illustrates the implementation process of this method, which integrates present advanced failure mode acquisition, failure mechanism analysis, failure effect analysis and quantitative criticality matrix analysis techniques together. A case is taken to illustrate the way of integration of these techniques and FMEA in detail.

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II. IMPLEMENTATION PROCESS OF INTEGRATED FMEA METHOD

Implementation process of integrated FMEA method is shown in Fig. 1. Seen from the figure, this new method add a variety of integrated simulation approach for new product in failure mode acquisition, failure mechanism analysis, failure effect analysis and criticality analysis process.

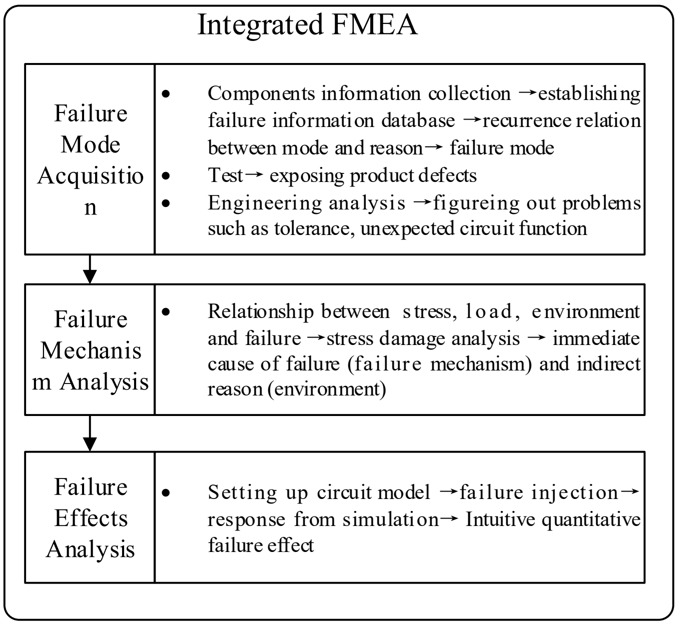

Figure 1. Implementation process of integrated FMEA method

A. *Failure Mode Acquisition Approaches*

1) Failure information database establishment

Electronic products are usually made of components, circuit boards, chassis, board-level interconnection, and interconnection between plate and the chassis structure. Although failure data and historical data of newly developed electronic products are scarce, there are a lot of failure mode related data of components available for reference. Failure mode, reason, mechanism and failure mode frequency ratio related data are collected to establish failure information database. Then failure modes of newly developed electronic product can be acquired through recurrence relations of mode, reason and next higher level effects among indenture levels, which is the only way to obtain failure modes information in FMEA when detailed design of product is completed without physical prototype or any experimental data.

Failure mechanism and failure mode frequency ratio in failure information database also can provide basis for failure mechanism analysis, effects analysis and criticality analysis.

2) Obtaining failure mode through test and engineering analysis

FMEA needs to constantly update in product design phase with repeated iteration. After product has physical prototype, a series of tests will be carried out, such as debugging, development test, Failure excitation test and reliability compliance test. Aiming at failure occurred in test, deep analysis should be taken to get new failure mode, reason and mechanism, and these data can be integrated into FMEA to assist new round of analysis.

For example, reliability enhancement test can accelerate failure mode exposure by improving the environment and stress. And failure reasons and mechanism obtained by analysis can be added to further analysis and saved into failure information database.

Acquiring failure mode by engineering analysis refers to take tolerance analysis and potential pathway analysis or other analysis for electronic products to find out tolerance, unexpected circuit function problems existing in overall design of products, and make clear failure modes caused by these problems.

B. *Failure Mechanism Analysis Approaches*

Failure mechanism analysis refers to take environment and stress simulation for product to obtain weak links and potential cumulative damage failure of product, and obtain failure mode, mechanism and reason of product according to the relationship between stress, environment, load and failure. Implementation process of failure mechanism analysis is shown in Fig. 2, which mainly includes modeling, stress analysis and damage analysis. Failure mechanism analysis not only can find out more failure modes, but also can directly give immediate causes (failure mechanism) and indirect reasons (environment factors) of failure modes.

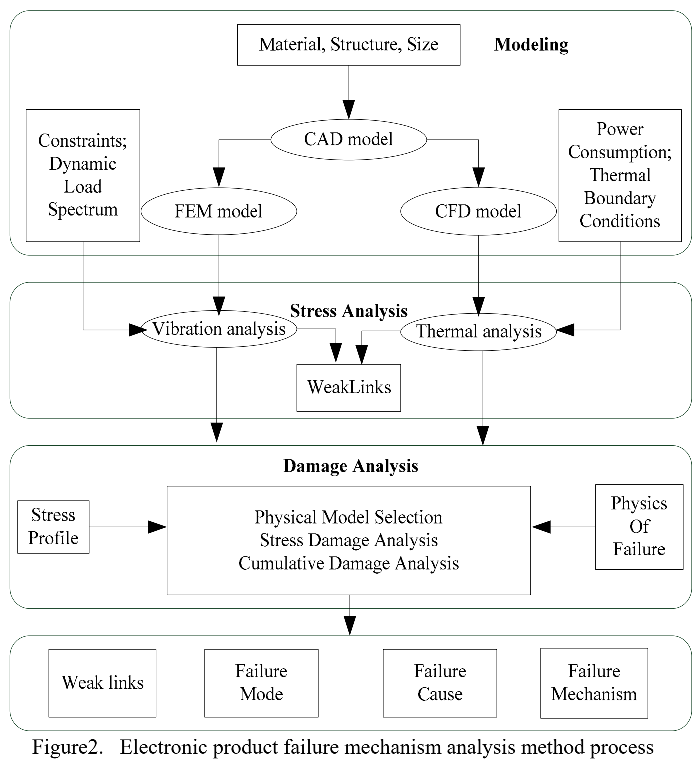

Figure2. Electronic product failure mechanism analysis method process

C. *Simulation-based Failure Effect Analysis Method*

The key of electronic products is the circuit. For the huge circuit system, it's not easy to determine how the failures in the lower layer units affect the upper layer circuit units. The simulation analysis method based fault injection can help designers determine ultimate failure effects of components and circuit.

The failure simulation analysis of electronic products can be divided into normal circuit simulation analysis and failure circuit simulation analysis. In normal circuit simulation analysis, a circuit model should be first built in EDA software, then the EDA simulation is carried out to obtain different level output responses in normal operating state. Similarly, a failure EDA model need to be established in the failure circuit simulation analysis first. The so-called failure EDA models refers the failure components other layer products models which are established according to failure modes. Then the failure circuit EDA model is formed by substituting failure EDA model for the corresponding components of normal circuit to obtain different level output responses in failure circuits. The effects of the injected failure modes can be acquired by comparing output responses in normal and failure conditions.

III. CASE STUDY

The implementation process of an integrated method for hardware FMEA of new electronic products is carried out with a case of avionics below.

A. System Definition

The electronic equipment is made up of the dual redundant channels (A, B channel) and a monitoring channel (C channel). The structure and function of A, B channel are identically same, including the power module, digital-analog converter (AC-DC) module, data processing module and CPU module. There are more than 200 categories and more than 2000 components in these four modules. The avionics is the initial agreement level; each circuit module is the agreement layer; component is the lowest agreement layer.

Temperature and vibration profile of the device are shown in Fig. 3 and Fig. 4.

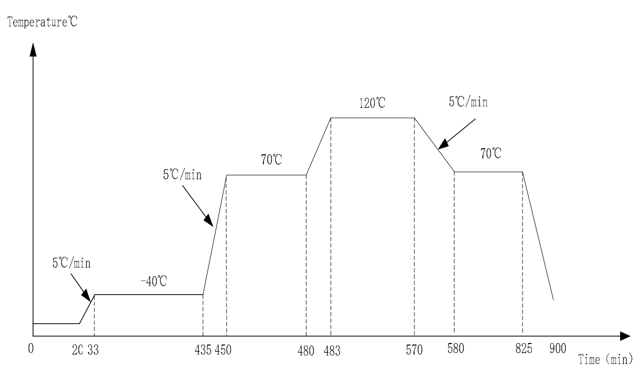

Figure 3. Temperature profile of the device

B. Failure Mode Acquisition

1) Failure information database establishment

It is necessary to collect much failure information of components at the beginning. The information in the database can be investigated from components handbook, GJB299C[22], Mil-HDBK-217F[23], RAC-FMD[5], FRACAS database, published data collection and reliability testing. The structure of the failure information database is shown in Fig. 5.

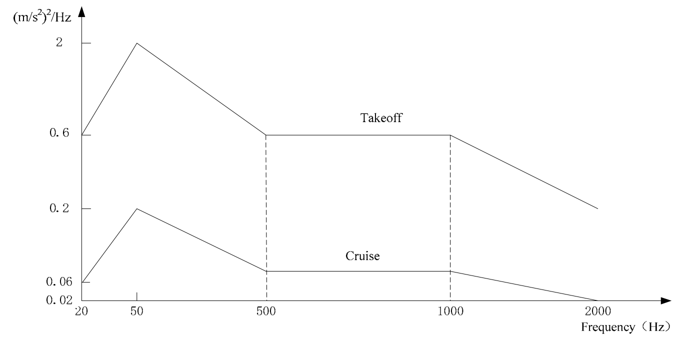

Figure 4. Vibration profile of the device

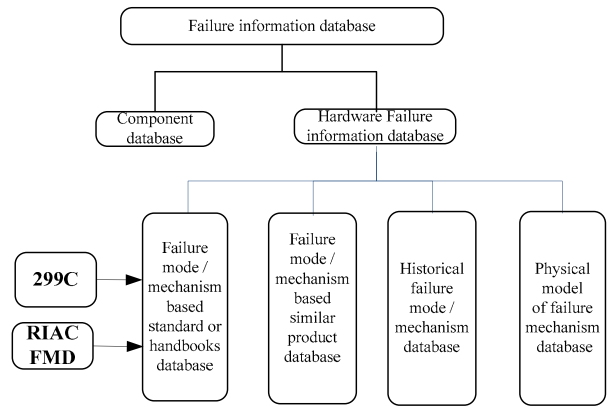

Figure 5. Structure of fault information database

2) Reliability enhancement test

Also, failure modes are also collected from reliability enhancement test. The low-temperature step-up-stress, high-temperature step-up-stress, vibration step-up-stress and the environmental stress are applied in reliability enhancement test of the device, which was exposed 10 kinds of failure. Then the designers analyzed the failure components to identify the cause, which was recorded in the FMEA table. Failure modes and causes from the reliability enhancement test are shown in Table I.

TABLE I. FAILURE MODES AND CAUSES FROM ENHANCEMENT TEST

Hardware	Failure modes	Failure cause	Stress
Pressure Sensor	Signal out-of-tolerance	Beyond the allowable temperature	low-temperature step-up-stress
Relays	Out failure	Low vibration resistance	vibration step-up-stress
DC-DC power	None output voltage	Pin fracture	Integrated stress
Flash chip	None output	Strong external stress	Integrated stress

C. *Failure Mechanism Analysis*

Three methods of thermal analysis, vibration analysis and stress damage analysis are implemented in failure mechanism analysis and the corresponding software are FloTHERM、ANSYS Workbench and CalcePWA.

1) *Thermal analysis*

In the thermal analysis, it's required to establish CFD model, generate meshing, enter the environment and load parameters and run the simulation under -40℃、70℃ and 120℃ according to the temperature profile shown in Figure 3 to get the corresponding temperature distribution of the device. Temperature distribution cloud picture of the device at 70℃ is shown in Fig. 6.

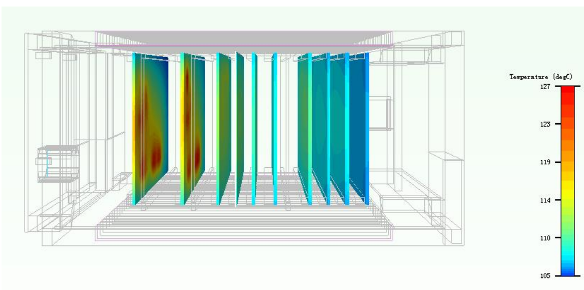

Figure 6. Temperature distribution cloud picture of the device

2) *Vibration analysis*

In vibration analysis, it's also required to establish FEM model, generate meshing, and respectively enter acceleration power spectral density in takeoff and cruising state according to Fig. 4, obtaining the root mean square value of acceleration cloud picture, root mean square value of displacement cloud picture and modal frequencies of the device. The root mean square value of acceleration and displacement cloud picture are respectively shown in Fig. 7 and Fig. 8.

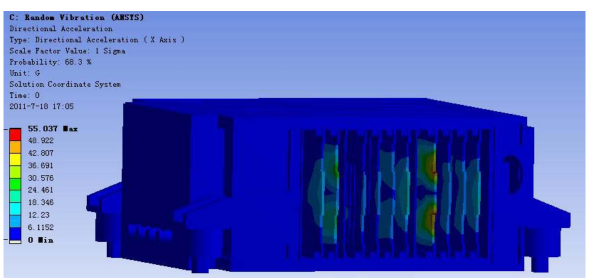

Figure 7. Root mean square value of acceleration cloud picture of the device at takeoff state

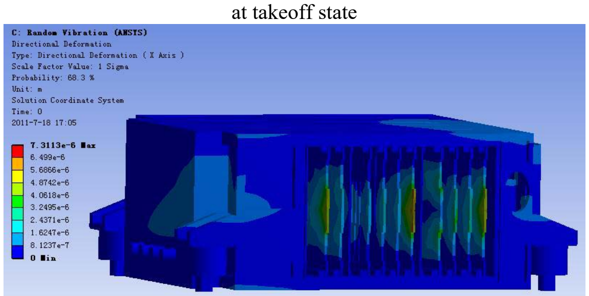

Figure 8. Root mean square value of displacement cloud picture of the deviceat takeoff state

3) *Damage stress analysis*

Establishing model in CalcePWA is the first step in damage stress analysis. And then make the board-level analysis of thermal and vibration to obtain the details of temperature and vibration responses of components. Finally enter temperature and vibration profile and operate failure prediction to obtain the life and corresponding failure mechanisms of components under temperature cycling and vibration cycling. When damage life is less than design life of the device, failures are considered to occur and failure modes are determined by failure mechanisms. As Fig. 9 shown, C20 and C22 which were marked by red are the failure points in the front of the AC-DC's PCB.

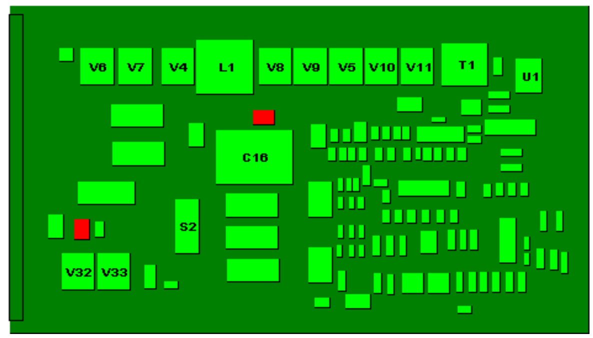

Figure 9. Failure point in the front of the AC-DC's PCB

There are two steps in the process of identification of the failure modes and failure causes. First, find out components of which temperature exceeds the allowance and components which are high vibration response and low damage life, then identify the above components as key components. Second, identify the failure modes and failure causes according to the load type of electronic products and the corresponding relations of damage mechanism, failure mode and failure cause.

D. *Failure Eeffect Analysis*

The EDA model of S1 signal processing circuit was establishment by Cadence software in the simulation-based failure effect analysis. The waveform of fault free circuit is shown in Fig. 10, in which the dotted line, dot-dash line and solid line sine respectively indicate the input waveform, the positive input waveform of voltage comparator and the approximate square output waveform of the voltage comparator.

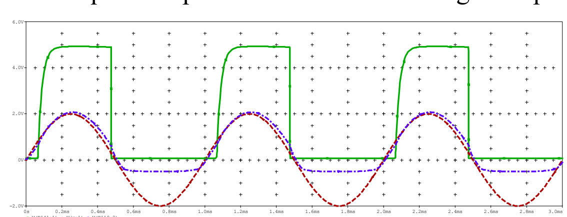

Figure 10. Simulation result of fault free circuit

C125 is a capacitance in the processing circuit. The first-order RC filter network is made up of C125 and R118. Simulation circuit schematic diagram of short fault effect analysis of C125 is shown in Fig. 11.

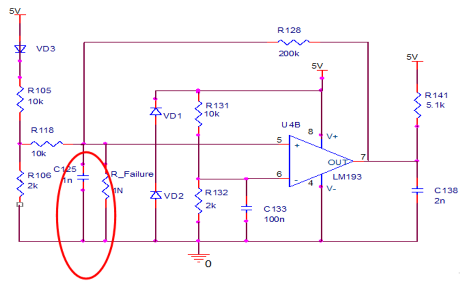

Figure 11. Simulation circuit schematic diagram of short fault effect analysis of C125

As illustrated in Fig. 11, the red circle indicates the position of the injected fault. Simulation results are shown in Fig. 12, in which the thick dashed indicates the input sine waveform. The thick solid line indicates input signal waveform of a voltage comparator positive. The thick solid line indicates output signal waveform of a voltage comparator. From the comparison between Fig. 10 and Fig. 12, when a short circuit occurs in C125, the signal cannot be input into the comparator, the signal processing circuit failing to process the signal.

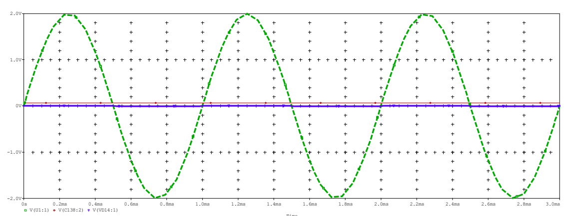

Figure 12. Simulation result of short fault effect analysis of C125

Analyze failure effect by EDA simulation to obtain failure effects of all layers. Table II below shows the failure effects of the part of failure modes in this case.

TABLE II. THE SAMPLE OF FAILURE EFFECT FROM FAILURE EFFECT ANALYSIS METHOD BASED ON SIMULATION

Component	Failure effect	Local influence	Effect of high layer	Ultimate Effect
C125 Capacitance	Open circuit	Open circuit on Capacitance	The signal processing circuit cannot filter out high frequency signal interference, and output signal easily beats	Equipment works in an unstable state
	Short circuit	Short circuit on Capacitance	The signal processing circuit cannot process the signal and the BIT function fails	The output signal of the device is incorrect

IV. CONCLUSIONS

This paper has provided an integrated method for hardware FMEA of new electronic products which integrates present advanced failure mode acquisition method, failure mechanism analysis method, failure simulation analysis method and quantitative criticality matrix analysis techniques considering backup design together. And the details of the implementation of this method has been presented by a case. This paper can draw the following conclusions:

(1) Failure information database establishment can solve the problem that failure mode of newly developed electronic products is scarce. Also it can provide the basic data for failure mechanism and failure criticality analysis;

(2) Failure modes, mechanisms and induced stress under the task environment can be obtained by failure mechanism analysis, which can provide the basis for improvement of the design.

(3)The method of simulation-based failure effect analysis can help designers quantitatively determine the failure effect of electronic components and circuit modules more objectively and accurately.

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